PATENT   ATTORNEY DOCKET NO. 114596-20-4009

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.:   09/434,394   Confirmation No.:   3898
Applicant: John S. Yates, Jr., et al.
Title: DETECTING REORDERED SIDE EFFECTS
Filed: November 4, 1999   I certify that this correspondence, along with any documents
Art Unit: 2122   referred to therein, is being transmitted by facsimile on February
Examiner: Nguyen Ba, H. V. A   28, 2005 to Art Unit 2122 at FAX no. 703 872 9306,
                                       Commissioner for Patents, P.O. Box 1450, Alexandria, VA
                                       22313-1450.
Atty. Docket: 114596-20-4009
Customer No.   38492
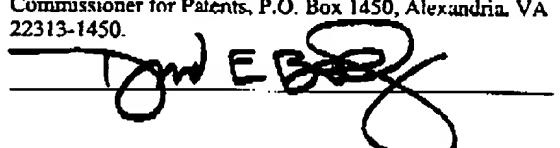
INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In accordance with 37 C.F.R. §§1.56, 1.97 and 1.98, Applicant wishes to make of record the items listed on the accompanying Form PTO-1449. Applicant respectfully requests the Examiner to fully consider the items and independently ascertain their teaching before issuance of the next action, and to make them of record in the file. The Examiner is also requested to initial and return a copy of the enclosed Form PTO-1449 to evidence such consideration.

1. Applicant has listed publication dates on the attached Form PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated. Applicant reserves the right to establish the patentability of the claims over any information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered. This Information Disclosure Statement should not be construed as a representation that information more material to the examination of this application does not exist.

2. The references listed on the enclosed Form 1449 are references that have come to light in applications listed in the Information Disclosure Statement of January 2001. For many of the listed references, pertinence is mentioned in the respective application file in which the reference came to light. Applicant has not reviewed all of them in detail. Of those that have been reviewed, none of the references are believed to be any more pertinent than the references provided in earlier IDS' and Forms 1449. However, in an abundance of caution, Applicant requests that they be considered.

Information Disclosure Statement   1   S/N 09/434,394
This paper dated February 28, 2005   2789410.1

PAGE 7/9 * RCVD AT 2/28/2005 11:25:20 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID: * DURATION (mm-ss):07-54

Application Serial No. 09/434,394
Atty. Docket No. 114596-20-4009

3. For items other than U.S. patents listed on the enclosed Form PTO-1449 for which a copy is not already made of record in this application, a copy was previously cited by or submitted to the Patent and Trademark Office in application Serial No. 09/239,194, filed January 28, 1999, Yates et al., Executing Programs for a First Computer Architecture on a Computer of a Second Architecture, in application Serial No. 09/322,443, filed May 28, 1999, Reese et al., Profiling of Computer Programs Executing in Virtual Memory Systems, or in application Serial No. 09/385,394, filed August 30, 1999, Yates et al., Computer for Executing Two Different Instruction Sets.

4. The non-patent references by Dean, Hank, Hookway and the three Intel non-patent references have been previously cited. They are cited again here with improved bibliographic information.

5. This Information Disclosure Statement it is being filed at a time when prosecution is closed, but may be reopened on withdrawal or reversal of all pending rejections. In the event of reopening of prosecution, entry of this Information Disclosure Statement is proper on payment of a fee pursuant to 37 C.F.R. §1.97(c)(2). Upon such entry, charge the fee due under C.F.R. §1.17(i)(1) to 23-2405, Order No. 114596-20-4009.

6. The Commissioner is hereby authorized to charge any additional fees that may be required for this Information Disclosure Statement, or credit any overpayment, to Deposit Account No. 23-2405, Order No. 114596-20-4009.

Respectfully submitted,

WILLKIE FARR & GALLAGHER LLP

Dated: February 28, 2005   By: _____
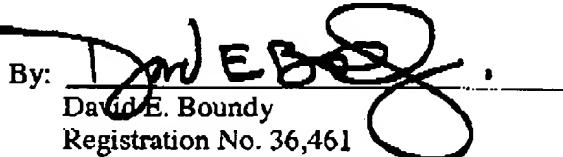
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FORM PTO-1449	U.S. DEPARTMENT OF COMMERCE	ATTY. DOCKET NO. 114596-20-4009	SERIAL NO. 09/434,394
	PATENT AND TRADEMARK OFFICE	APPLICANT John S. Yates, Jr., et al.	
INFORMATION DISCLOSURE CITATION			
(Use several sheets if necessary)		FILING DATE November 4, 1999	GROUP ART UNIT 2122

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
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		5,404,473	04/04/1995	Papworth	712	241	Mar. 1, 1994
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		Dean, ProfileMe: Hardware Support for Instruction-Level Profiling on Out-of-Order Processors," Proceedings of 30th Annual Intl. IEEE/ACM Symp. on Microarchitecture, pp. 292-302 (Dec. 1997)
		R.E. Hank, et al., "Region-Based Compilation: An Introduction and Motivation" Proceedings of the 28th Annual International Symposium on Microarchitecture, pp. 158-168 (Dec. 1995)
		Raymond J. Hookway, Mark A. Herdeg, Digital FX!32: Combining Emulation and Binary Translation (August 28, 1997), http://www.digital.com/info/DTJP01HM.HTM
		Intel Corporation, Intel Architecture Software Developer's Manual, Volume 1: Basic Architecture, pages 3-10 to 3-13, 7-1 to 7-3, 7-20 to 7-25; Volume 2: Instruction Set Reference, pages 3-60 to 3-63, 3-240 to 3-251; Volume 3: System Programming Guide, pages 11-1 to 11-3, 11-10 to 11-13, 14-1 to 14-3, 14-10 to 14-15 (1997)
		Intel Corporation, Pentium Processor Family Developer's Manual (1997), pages 1-1 to 1-6, 2-1 to 2-20
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EXAMINER	DATE CONSIDERED

2789410.1